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10/523,727	09/07/2006	John M. Shannon	GB03 0105 US	1094

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
370 W. TRIMBLE ROAD MS 91/MG
SAN JOSE, CA 95131

EXAMINER	
PHINAZEE, SIDNEY S	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,727	SHANNON ET AL.	
	Examiner	Art Unit	
	SIDNEY PHINAZEE	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2-04-05* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2-4-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is the initial first office action in reference to application (10/523727), in which claims 1-27 are taken under consideration at this time.

Claim 8 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim cannot depend from another multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claim 8 has not been further treated on the merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The recitation "any claim 20" is vague and indefinite.

Claim 23 is objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim does not refer back in the alternative only. See MPEP § 608.01(n). Accordingly, the claim 23 has not been further treated on the merits.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7,9-22,24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Hebiguchi (5,801,398).

Regarding claim 1, Hebiguchi discloses an insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising: a semiconductor body layer (54); a source electrode (45) extending across a source region of the semiconductor body layer (54) defining a Schottky potential barrier between the source electrode (45) and the source region of the semiconductor body layer (54) a drain electrode (46) connected to the semiconductor body layer; and a gate electrode (42) for controlling transport of carriers of the predetermined carrier type from the source electrode (45) to the source of the semiconductor body layer (54) across the barrier when the source region is depleted; wherein the gate electrode (42) is arranged in an overlapping relationship to the source electrode on the opposite side of the semiconductor body layer to the source electrode having a gate insulator layer (43) between the gate electrode and the semiconductor body layer; and the gate electrode (42) is spaced from the source electrode (45) by at least the combined full thickness of the semiconductor body layer (54) and the gate insulator (43) over the whole of the gate-controlled region of the Schottky barrier. (Fig 2 and 4)

As pertains to claim 2, Hebiguchi discloses an insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising: a semiconductor body layer (54) having a thickness of at least 10 nm; a source electrode (22) extending across a source region of the semiconductor body layer (54) defining a potential barrier between the source electrode (45) and a source region of the

semiconductor body layer (54), a drain electrode (46) connected to the semiconductor body layer; and a gate electrode (42) for controlling transport of carriers of the predetermined carrier type from the source electrode (45) to the source region of the semiconductor body layer (54) across the barrier when the source region is depleted; wherein the gate electrode (42) is arranged in an overlapping relationship to the source electrode on the opposite side of the semiconductor body layer 5 to the source electrode having a gate insulator layer (43) between the gate electrode and the semiconductor body layer; and the gate electrode (42) is spaced from the source electrode by at least the combined thickness of the full thickness of the semiconductor body layer (54) and the gate insulator (43) over the whole of the gate-controlled region of the source barrier.

Regarding claim 2 it would have been obvious to one having ordinary skill in the art at the time of the invention was made to incorporate the dimension, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. [In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA1980)]

Regarding claim 3 Hebiguchi teaches dopant impurities (column 11 lines 24-33) in the semiconductor body layer under the source electrode for controlling the effective barrier height.

Regarding claim 4 Hebiguchi discloses wherein the dopant is a shallow implant of donor impurities to raise the effective barrier height to holes and to lower the effective barrier height to electrons.

As pertains to claim 5, Hebiguchi discloses a field relief structure (54') at the lateral edge of the source electrode facing the drain electrode.

Regarding claim 6, Hebiguchi teaches wherein the drain electrode (46) is connected to a drain region of the semiconductor body layer (54), the drain region being spaced from the source region by an intermediate region of the semiconductor body layer (54), and the field relief structure is the intermediate region of the semiconductor body layer between the source region (45) and the drain region, the intermediate region being compensated.

Regarding claim 7, Hebiguchi discloses A transistor according to claim 5 wherein the drain electrode (85) is connected to a drain region of the semiconductor body layer (81), the drain region being spaced from the source region by an intermediate region of the semiconductor body layer (81), and the field relief structure comprises an extension (81') to the source electrode extending laterally across at least part of the intermediate region, separated from the said part of the intermediate region by a field relief insulating layer (82).(Fig 5)

Regarding claim 9, Hebiguchi teaches wherein the lateral extent of the gate electrode (42) towards the drain is overlapped wholly by the source electrode (45).

Regarding claim 10, Hebiguchi teaches a pair of drain electrodes (102) and corresponding drain regions of the semiconductor body layer (98) laterally on either side of the source region. (Fig 15)

Regarding claim 11, Hebiguchi teaches wherein the potential barrier has a barrier potential for the predetermined charge carrier type of between 0.25 times and 0.75 times the band gap of the semiconductor of the semiconductor body layer.

Regarding claim 11 It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the dimension into the process of the device, since it has been held that where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. [In re Woodruff, 919 F.2d 1575, 1578, 16USPQ2d 1934, 1936 (Fed. Cir. 1990)]

Regarding claim 12, Hebiguchi teaches a heterojunction layer (71) between the source electrode and the semiconductor body layer forming the barrier.

Regarding claim 13, Hebiguchi teaches wherein the semiconductor body layer (54) is a thin film of deposited semiconductor material

Regarding claim 14, Hebiguchi discloses wherein the semiconductor layer (54) is of amorphous silicon.

Regarding claim 15 and 16 applicant has noted in the specification that the material is well known in the art. Since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. [In re Leshin, 125 USPQ 416]

Regarding claim 17, Hebiguchi discloses an insulated gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising: a semiconductor body layer (54); a laterally-extending source electrode (45) defining a

lateral barrier at one major side of the semiconductor body layer (54); a drain electrode (46) laterally spaced along the semiconductor body layer from the source electrode (45) by an intermediate region of the semiconductor body layer; a gate electrode (42) extending laterally on the opposite major side of the semiconductor body layer (54) to the source electrode (45) to define a gate-controlled region of the semiconductor body layer extending across the semiconductor body layer to the source barrier; a gate insulator layer (43) between the gate electrode (42) and the semiconductor body layer (54); and a field relief structure (54') on the edge of the source region facing the drain region.

Regarding claim 18, Hebiguchi discloses an insulated-gate transistor for conduction using charge carriers of a predetermined conductivity type, comprising: a semiconductor layer (54) that provides a body portion of the transistor between a source of the said carriers and a drain for the said carriers; and an insulated gate including a gate electrode (42) coupled to the body portion via an intermediate gate-dielectric layer (43); wherein the source comprises a barrier to the said carriers between a source electrode (45) and the semiconductor layer (54) so as to inhibit carrier flow from the source into the body portion except as controlled by the insulated gate; the source and the insulated gate are located at respective opposite major sides of the semiconductor layer (54) in an opposed laterally-overlapping relationship which separates the source from the insulated gate by at least an intermediate thickness of the semiconductor layer (54); and the laterally-overlapping insulated gate is coupled to the source barrier via the intermediate thickness of the semiconductor layer so as to permit transistor conduction

by controlled emission of said carriers across the source barrier by voltage applied between the gate and source electrodes upon depletion of the body portion across the intermediate thickness of the semiconductor layer (54) from the insulated gate. Further, in regard to the claimed functional language, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Regarding claim 19, Hebiguchi discloses a transistor comprising a source electrode (45) on the opposite side of a semiconductor body layer (54) to an insulated gate electrode (42), and a drain electrode (46) connected to the semiconductor body layer (54), wherein the source electrode has a potential barrier to the semiconductor body layer, and source- drain current is controlled by the gate voltage upon depletion of a region of the semiconductor body layer adjacent to the source barrier by the application of suitable source-drain voltage and gate voltage.

Regarding claim 20, Hebiguchi discloses using a transistor including applying a voltage between the source (45), gate (42) and drain electrode (46) to substantially deplete the whole of the source region of the semiconductor body layer (54) in the region of the gate electrode and to cause carriers of the predetermined conductivity type to be emitted by the source electrode across the barrier and across the depleted source region to the drain region and then to the drain electrode. Also it has been held that a recitation with respect to manner in which a claimed apparatus is intended to be

employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. [Ex parte Masham, 2 USPQ2d 1647 (1987)]. Likewise claim 21 is rejected.

Regarding claim 21, Hebiguchi teaches the use of a transistor including varying the source-gate voltage to vary the source-drain current.

Regarding claim 22, Hebiguchi discloses a transistor arrangement comprising a substrate (90); and a plurality of transistors distributed over the substrate.

As pertains to claim 24, Hebiguchi teaches a transistor arrangement wherein there is a shallow implant of donor impurities under the barriers of p-type and n-type transistors to raise the effective barrier height to holes in the p-type transistors 2o and to lower the effective barrier height to electrons in the n-type transistors.

As pertains to claim 25, Hebiguchi teaches a transistor circuit, including an insulated gate field effect transistor having a semiconductor body layer (54), a source electrode (45) and a gate electrode (42) arranged in opposed relationship on opposite sides of the semiconductor body layer (54), with a barrier between the source electrode and the semiconductor body layer and a gate insulator (43) between the semiconductor body layer and the gate, and a drain electrode (46) connected to the semiconductor body layer (54); and a circuit (abstract) arranged to apply voltages to source, gate and drain electrodes to deplete the semiconductor body layer in the region of the source electrode and to control the barrier height of the barrier by the source-gate voltage to control the emission of carriers from the source electrode to the semiconductor body layer and hence to control the source-drain current by the source-gate voltage.

Regarding claim 26, Hebiguchi teaches a method of operating a transistor having a source electrode (45), a drain electrode (46), a semiconductor body layer (54) having a source region in contact with the source electrode (45) and a drain region in contact with the drain electrode (46), and an insulated gate (42) opposed to the source electrode (45), the method including: applying a voltage between the source, gate and drain to substantially deplete the whole of the source region of the semiconductor body layer and to cause carriers to be emitted by the source electrode across the barrier and across the depleted source region to the drain region and then to the drain electrode. There is no exact range of depletion magnitude to differentiate the claimed "substantially depleted" recitation from the inherent depletion of the Hebiguchi channel during operation. In other words, "substantially" is considered broad and in no way distinguishes over Hebiguchi. The claimed method of operating is fundamental in that it basically states apply a gate, source, and drain voltage to operate the device. There is no novelty in this fundamental method because "substantially" is broad and does not distinguish over normal operation of the prior art device (Hebiguchi). Claim 27 is likewise rejected. There is no magnitude of depletion to distinguish over the depletion present in Hebiguchi.

Regarding claim 27, Hebiguchi teaches a method including holding the source-drain voltage at a value that depletes the source region and varying the source-gate voltage to control the current flowing from source to drain.

As regards to the invention, it has been held that a recitation with respect to manner in which a claimed apparatus is intended to be employed does not differentiate

the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. [Ex parte Masham, 2 USPQ2d 1647 (1987)]

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SIDNEY PHINAZEE whose telephone number is (571)270-5020. The examiner can normally be reached on Mon-Fri 7:30-5:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SSP

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815